CLAIMS

We claim:

1. A memory cell, comprising:

a first NMOS transistor having a source, drain and gate; and

a first PMOS transistor having a source, drain and gate, the gate of the PMOS transistor being coupled to a floating gate region and the gate of the first NMOS transistor, and the drain of the PMOS transistor coupled to the drain of the first NMOS transistor,

wherein at least one of the first NMOS transistor and first PMOS transistor includes a three-implant channel region to reduce the threshold voltage of the transistor.

2. A memory cell, comprising:

a first NMOS transistor having a source, drain and gate; and

a first PMOS transistor having a source, drain and gate, the gate of the PMOS transistor being coupled to a floating gate region and the gate of the first NMOS transistor, and the drain of the PMOS transistor coupled to the drain of the first NMOS transistor;

wherein the first NMOS transistor and first PMOS transistor each include a three-implant channel region to reduce the threshold voltage of the transistors.

3. A memory cell, comprising:

a first NMOS transistor having a source, drain and gate;

a first PMOS transistor having a source, drain and gate, the gate of the PMOS transistor being coupled to a floating gate region and the gate of the first NMOS transistor, and the drain of the PMOS transistor coupled to the drain of the first NMOS transistor; and

a second NMOS transistor, having a drain coupled to a tunnel capacitor, the output of the tunnel capacitor coupled to the floating gate region,

wherein the first NMOS transistor and first PMOS transistor each include a three-implant channel region to reduce the threshold voltage of the transistors.

4. The cell of claim 3 wherein the second NMOS transistor includes a two-implant channel region.

5. The cell of claim 4 wherein the first NMOS transistor and PMOS transistor are formed with a first, second and third successive implants in their channel regions, and the second NMOS transistor does not include the first implant in its channel region.

6. The cell of claim 3 wherein the first implant for the first NMOS transistor comprises boron having a concentration of 3×10^{12} atm/cm^2.

7. The cell of claim 3 wherein the first implant for the first PMOS transistor comprises phosphorous having a concentration of about 8×10^{12} atm/cm^2.

8. The cell of claim 3 wherein the first PMOS transistor three-implant region further includes:

a region of phosphorous at an at a concentration of 4×10^{12} atm/cm^2;

a region of arsenic at a concentration of 4×10^{12} atm/cm^2; and

a region of phosphorous at having an impurity concentration of 3.2×10^{12} atm/cm^2.

9. The cell of claim 3 wherein the first NMOS transistor three-implant region includes:

a first region of boron having an impurity concentration of 4.4×10^{12} atm/cm^2;

a second region of boron having an impurity concentration of 4×10^{12} atm/cm^2; and

a third region of BF_2 having an impurity concentration of 3.2×10^{12} atm/cm^2.